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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,087	01/14/2004	Arup Bhattacharyya	MI22-2473	2443

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,087	BHATTACHARYYA, ARUP	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *71-73,76 and 78-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *71-73,76 and 78-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/18/06 has been entered.

Response to Amendment

Amendment filed 4/18/06 with said RCE forms the basis for this office action. In said Amendment applicant substantially amended all pending claims 71-73, 76 and 78-81; claims 1-70, 74, 75, 77 and 82-88 had previously been cancelled.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 71*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al (6,888,750 B2) in view of Sugahara (5,006,913) (made of record by IDS).

Walker et al teach a computer system (col. 1) (e.g., logic circuits (Figures 12-14) together with the nonvolatile memory array (see "Field of Invention") constitute a computer system) with stacking either according to the embodiment of Figures 10 or the embodiment of Figure 11) comprising: a signal source capable to provide a data signal (from word line 445; col. 17, lines 60-65); and an inverter 443 coupled with the signal source (col. 17, l. 45-46), capable to invert the data signal and output the inverted signal (through bit lines 447); the inverter including (Figure 11);

a structure comprising semiconductor material (structure being either 413/418 or 413) (Figure 11);

a first transistor (PMOS TFT; Figure 11) supported by the structure, the first transistor comprising a first gate 409 (Figure 11) and first active region (in 425 between source/drain regions 429) (Figure 11) proximate the first gate; the first active region including a first channel region (=region between neighboring s/d regions 429) and a pair of first source/drain regions 429; at least a portion of the first active region being within the structure (Figure 11), the first transistor being a PFET and the first source/drain regions accordingly being p-doped regions (Fig.11);

a material layer over at least a portion of the first transistor (407 e.g.) (Fig.11);

a second transistor over the material layer and comprising a second gate 405 and a pair of second source/drain regions 417 (Fig.11), the second transistor being an NFET (NMOS TFT)) (Figure 11) and the second source/drain regions accordingly being n-type doped regions; the first and second gates being electrically connected to one another (col. 14, l. 47-57), and being in electrical connection with the signal source

471(Figure 14); and one of the first source/drain regions being electrically connected to one of the second source/drain regions and being in electrical connection with the output (Figure 14).

Walker et al do not necessarily teach the limitation that an insulative material over at least a portion of the first transistor, a first layer of semiconductive material over the insulative material, and a second layer semiconductive material over the first one, the second layer physically contacting the first and being compositionally different from the first.

However, it would have been obvious to include said limitation in view of Sugahara et al, who, in a patent on stacked semiconductor devices, hence analogous art, teach stacking with an insulative layer 10 in between the field effect transistors so as to mitigate mechanical stress between otherwise abutting layers of different CTE (see abstract). It would be obvious to include the teaching by Sugahara et al because $TiSi_x$ and polysilicon have widely different coefficients of thermal expansion, considering the metallic nature of $TiSi_x$ and the well-known Wiedemann-Franz Law.

2. ***Claims 72-73, 76 and 80*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al and Sugahara et al as applied to claim 71 above, and further in view of Bulsara et al (US 2003/0030091 A1).

As detailed above, claim 71 is unpatentable over Walker et al in view of Sugahara et al. Neither necessarily teach the further limitations defined by claims 72, 73 or 76.

However, it would have been obvious to include said limitations in view of the teaching as prior art by Bulsara et al that relaxed silicon-germanium including a strained

layer 18 ([0036]) (i.e., layer with strained lattice, hence inherently crystalline in addition to being strained) and a relaxed underlying silicon-germanium (claim 80) crystalline layer 14 ([0035]) (with from 20 to 90 % germanium, hence claim 81 is met because there necessarily is one % value contained in the claimed range) directly applied on a graded silicon-germanium (SiGe) layer 12 (loc.cit.) (i.e., on top of a crystalline silicon-containing layer (inherently crystalline, because without being crystalline here cannot be a grading of the lattice constant (see [0003]) so as to produce field effect transistors (FETs) with increased channel mobility, hence improved device speed (loc.cit.) Implementation of the teaching for both the NFET and the PFET by Walker et al necessarily leads to the claimed device because the source/drain regions in Walker et al extend throughout the entire silicon substrate, being members of a poly bit line 333 (see Figure 11 and Figure 10A, and see column 13, lines 20-28).

Motivation to include the teaching by Bulsara et al in the invention by Walker et al derives at least from the resulting improvement in device speed as taught by Bulsara (loc.cit.).

3. ***Claims 78 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al, Sugahara et al and Bulsara et al as applied to claim 72 above, and further in view of Hsu et al (6,793,731 B1).

As detailed above, claim 72 is unpatentable over Walker et al in view of Sugahara et al and Bulsara et al, none necessarily teaching the further limitation defined by claim 78 or claim 79. However, said limitations would have been obvious over Hsu et al, who teach

as prior art polycrystalline SiGe (cols. 1-2), while teaching as improvement thereof single-crystal relaxed SiGe free of defects (abstract and col. 2, l. 65 – col. 5, l. 65). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

Response to Arguments

Claims have been substantially amended and arguments in traverse only rely on the amended portions. New art has been found and herewith is presented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
June 12, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)